**Amendment to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1.- 12. (Canceled)

13. (New) A method for recovering a digital data signal ($D_{out}$) and a clock signal ($Ck_{out}$) comprising:

receiving a data signal including a plurality of successive bits;

generating, from the data signal, the clock signal ($Ck_{out}$) with a resonator circuit;

phase locking the clock signal ($Ck_{out}$) to the data signal by measuring a phase difference between the clock signal ($Ck_{out}$) and the data signal and by time delaying the clock signal ($Ck_{out}$) in response to the phase difference;

sampling the data signal at approximately the center of each bit with the clock signal ($Ck_{out}$); and

generating, as a result of the sampling, the digital data signal ($D_{out}$).

14. (New) The method of claim 13, delaying the clock signal ($Ck_{out}$) further comprising:

generating a first steering signal based on the phase difference between the clock signal ($Ck_{out}$) and the data signal; and

controlling, with the first steering signal, a controlled delay unit.

15. (New) The method of claim 13 further comprising:

generating a second steering signal based on the frequency difference between the clock signal ($Ck_{out}$) and an output signal from the resonator circuit;

controlling, with the second steering signal, a controlled oscillator in a frequency locked loop; and

frequency locking the clock signal ($Ck_{out}$) to the output of the resonator circuit.

16. (New) The method of claim 15 further comprising:

filtering the first steering signal with a first low pass filter; and

filtering the second steering signal with a second low pass filter.

17. (New) The method of claim 16 wherein a cut-off frequency of the first low pass filter is approximately 10 to 20 times smaller than the cut-off frequency of the second low pass filter.

18. (New) The method of claim 16 wherein a cut-off frequency of the first low pass filter is between 1 KHz and 50 KHz and a cut-off frequency of the second low pass filter is between 40 KHz and 2 MHz.

19. (New) The method of claim 13 wherein a data rate of the data signal is 622 MHz, 2.5 GHz, or 10 GHz.

20. (New) A circuit to recover a digital data signal ($D_{out}$) and a clock signal ($Ck_{out}$) from a received data signal ($D_{in}$), the received data signal ($D_{in}$) including a plurality of successive bits, the circuit comprising:

a resonator circuit to generate a clock signal from the received data signal ($D_{in}$) and to generate the digital data signal ($D_{out}$) by sampling the received data signal ($D_{in}$) with the clock signal ($Ck_{out}$),

a phase detector to measure a phase difference between the clock signal ($Ck_{out}$) and the received data signal ($D_{in}$) and to phase lock the clock signal ($Ck_{out}$) and the received data signal ($D_{in}$) by time delaying the clock signal ($Ck_{out}$) depending on the phase difference; and

a controlled delay unit to delay the clock signal ($Ck_{out}$) depending on the phase difference to sample the received data signal ($D_{in}$) at approximately the center of each bit.

21. (New) The circuit of claim 20, the controlled delay unit to generate the time delay in response to a first steering signal, the first steering signal based on the phase difference between the clock signal ($Ck_{out}$) and the received data signal ($D_{in}$)

22. (New) The circuit of claim 21 further comprising:

a frequency locked loop to frequency lock the clock signal and an output of the resonator circuit, the frequency locked loop including a controlled oscillator, the controlled oscillator to respond to a second steering signal, wherein the second

steering signal is based on a frequency difference between the clock signal ($Ck_{out}$) and an output signal from the resonator circuit.

23. (New) The circuit of claim 22 further comprising:

a first low pass filter to filter the first steering signal; and

a second low pass filter to filter the second steering signal.

24. (New) The circuit of claim 23 wherein a cut-off frequency of the first low pass filter is approximately 10 to 20 times smaller than the cut-off frequency of the second low pass filter.

25. (New) The circuit of claim 23 wherein a cut-off frequency of the first low pass filter is between 1 KHz and 50 KHz and a cut-off frequency of the second low pass filter is between 40 KHz and 2 MHz.